a1 cont SILA:098, titled "DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods."

In the Claims:

Please cancel claim 2 and add new claims 3-40.

The rewritten clean versions of all the pending claims are provided below. Attached at the end of this paper is an Appendix providing an indication of the changes relative to the prior version of the claims, as now required by Rule 121(c).

(AMENDED)

1. A receiver digital circuitry, comprising:

digital down-converter circuitry configured to mix a digital input signal provided by a receiver analog circuitry with a digital intermediate frequency (IF) local oscillator signal to generate a digital down-converted signal; and

digital filter circuitry configured to filter the digital down-converted signal to generate a filtered digital signal,

wherein the digital filter circuitry provides a notch at a frequency that corresponds to a residual DC offset of the receiver analog circuitry.

a2

3. The receiver digital circuitry of claim 1, wherein the digital filter circuitry provides the notch at minus a frequency of the intermediate frequency local oscillator signal.

4. The receiver digital circuitry of claim 3, wherein the digital filter circuitry provides the notch by using a notch filter circuitry.

5. The receiver digital circuitry of claim 4, wherein the notch filter circuitry has one or more poles the locations of which are adjustable over an adjustment cycle of the notch filter circuitry.

6. The receiver digital circuitry of claim 5, wherein the locations of the one or more poles of the notch filter circuitry are adjusted in an initial part of the adjustment cycle of the notch filter circuitry so that the notch filter circuitry tends to settle quickly.

7. The receiver digital circuitry of claim 6, wherein the locations of the one or more poles of the notch filter circuitry are further adjusted in a latter part of the adjustment cycle of the notch filter circuitry so that the notch filter circuitry tends to produce a narrow notch.

8. The receiver digital circuitry of claim 7, wherein the locations of the one or more poles of the notch filter circuitry are adjusted by modifying at least one filter coefficient of the notch filter circuitry.

9. The receiver digital circuitry of claim 8, wherein the locations of the one or more poles of the notch filter circuitry are adjusted before a reception of a burst of data by the receiver digital circuitry begins.

10. The receiver digital circuitry of claim 9, wherein the intermediate frequency local oscillator signal comprises a digital signal.

11. The receiver digital circuitry of claim 10, wherein the digital filter circuitry further comprises:

a cascade integrator/comb filter circuitry configured to receive and filter the digital down-converted signal, the cascade integrator/comb filter circuitry

further configured to provide a cascade integrator/comb filter circuitry output signal; and

a secondary filter circuitry configured to receive and filter the cascade integrator/comb filter circuitry output signal, the secondary filter circuitry further configured to provide the filtered digital signal.

12. The receiver digital circuitry of claim 11, wherein the secondary filter circuitry further comprises the notch filter circuitry and at least one biquad filter circuitry configured to receive and filter an output signal of the notch filter circuitry.

13. The receiver digital circuitry of claim 12 used in a radio-frequency transceiver circuitry.

14. A radio-frequency (RF) receiver circuitry, comprising:

receiver analog circuitry included within a first integrated circuit, the receiver analog circuitry configured to receive and process a radio-frequency input signal to generate a processed radio-frequency signal, the receiver analog circuitry further configured to use an analog-to-digital converter circuitry to convert the processed radio-frequency signal into a digital output signal; and

receiver digital circuitry, included within a second integrated circuit and coupled to the receiver analog circuitry within the first integrated circuit, the receiver digital circuitry configured to receive and process the digital output signal to generate a processed digital signal, the receiver digital circuitry further configured to provide a notch in a frequency spectrum of the processed digital signal,

wherein the receiver digital circuitry provides the notch at a frequency that corresponds to a residual DC offset of the receiver analog circuitry.

15. The radio-frequency receiver circuitry of claim 14, wherein the receiver digital circuitry further comprises a notch filter circuitry configured to provide the notch.

16. The radio-frequency receiver circuitry of claim 15, wherein the notch filter circuitry provides the notch at minus a frequency of an intermediate frequency local oscillator signal.

17. The radio-frequency receiver circuitry of claim 16, wherein the notch filter circuitry has one or more poles the locations of which are adjustable so as to modify the settling time and notch width of the notch filter circuitry.

18. The radio-frequency receiver circuitry of claim 17, wherein the locations of the one or more poles of the notch filter circuitry are adjusted at an initial point in time so that the notch filter circuitry tends to settle quickly.

19. The radio-frequency receiver circuitry of claim 18, wherein the locations of the one or more poles of the notch filter circuitry are adjusted at least once more after the initial point in time so that the notch filter circuitry tends to produce a progressively narrow notch.

20. The radio-frequency receiver circuitry of claim 19, wherein the locations of the one or more poles of the notch filter circuitry are adjustable by modifying at least one filter coefficient of the notch filter circuitry.

21. The radio-frequency receiver circuitry of claim 20, wherein adjustment of the locations of the one or more poles of the notch filter circuitry completes before a reception of a burst of data by the receiver digital circuitry begins.

22. The radio-frequency receiver circuitry of claim 21, wherein the intermediate frequency local oscillator signal comprises a digital signal.

23. The radio-frequency receiver circuitry of claim 22, used within a radio-frequency transceiver circuitry.

24. The radio-frequency receiver circuitry of claim 22, further comprising digital programmable gain amplifier circuitry configured to apply a programmable gain to the processed digital signal to produce a scaled digital signal.

25. The radio-frequency receiver circuitry of claim 24, further comprising a baseband processor circuitry coupled to the receiver digital circuitry, the baseband processor circuitry configured to receive the scaled digital signal.

26. The radio-frequency receiver circuitry of claim 25, used within a radio-frequency transceiver circuitry.

27. The radio-frequency receiver circuitry of claim 24, further comprising digital-to-analog converter circuitry configured to convert the scaled digital signal to an analog signal.

28. The radio-frequency receiver circuitry of claim 27, further comprising a baseband processor circuitry coupled to the receiver digital circuitry, the baseband processor circuitry configured to receive the analog signal.

29. The radio-frequency receiver circuitry of claim 28, used within a radio-frequency transceiver circuitry.

30. A method of receiving a radio-frequency (RF) signal, comprising:
receiving and processing the radio-frequency signal to generate an analog processed radio-frequency signal;
converting the analog processed radio-frequency signal to a digital signal; and
processing the digital signal by providing a notch at a frequency that corresponds to a residual DC offset in the analog processed radio-signal.

31. The method of claim 30, wherein processing the digital signal comprises providing the notch at minus a frequency of an intermediate frequency local oscillator signal.

32. The method of claim 31, wherein providing the notch includes using a notch filter circuitry that has one or more poles the locations of which are adjustable so as to modify the settling time and notch width of the notch filter circuitry.

33. The method of claim 32, wherein providing the notch further includes adjusting the locations of the one or more poles of the notch filter circuitry at an initial point in time so that the notch filter circuitry tends to settle quickly.

34. The method of claim 33, wherein providing the notch further comprises adjusting the locations of the one or more poles of the notch filter circuitry at least once more after the initial point in time so that the notch filter circuitry tends to produce a progressively narrow notch.

35. The method of claim 34, wherein providing the notch further comprises adjusting the locations of the one or more poles of the notch filter circuitry by modifying at least one filter coefficient of the notch filter circuitry.

36. The method of claim 35, wherein providing the notch further comprises completing the adjustment of the locations of the one or more poles of the notch filter circuitry before a reception of a burst of data by the receiver digital circuitry begins.

37. The method of claim 36, further comprising applying a programmable gain to the processed signal to produce an scaled digital signal.

38. The method of claim 37, further comprising providing the scaled digital signal to a baseband processor circuitry.

39. The method of claim 37, further comprising converting the scaled digital signal to an analog signal.

40. The method of claim 39, further comprising providing the analog signal to a baseband processor circuitry.

CONCLUSION

With this amendment, claims 1 and 3-40 are pending. Claim 2 has been cancelled. A check in the amount of $342.00 is enclosed for the addition of 19 dependent claims.

Should any fees under 37 CFR 1.16-1.21 be required for any reason relating to the enclosed materials, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/SILA:097. The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,

Maximilian R. Peterson
Registration No. 46,469
Attorney for Applicant

O'KEEFE, EGAN & PETERMAN, L.L.P.
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
512-347-1611
512-347-1615 (Fax)